CMOS LARGE SIGNAL MODEL FOR CAD

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ABSTRACT — **A compact large-signal model for high frequency CMOS transistors is proposed and experimentally evaluated with DC, S-parameter Power Spectrum measurements and load pool measurements. Very good correspondences between measurements on 100 nm CMOS FETs (f_T = 140 GHz, f_{max} =100 GHz) and simulations were achieved. Due to the low number of model parameters and the careful selection of model equations, the model exhibits excellent convergence behavior, a property important for successful nonlinear circuit simulation of RF circuits.**

INTRODUCTION

In recent years the RF performance of CMOS transistors has been dramatically improved. Today, a state of the art CMOS technology offers a very high frequency of operation, thus becoming a cheap technology for microwave applications. A significant amount of work has been done in the field of CMOS transistor modeling and parameter extraction [1-6]. However, many models implemented in software packages are excessively detailed, resulting in a huge number of model parameters. Because of this, and the fact that *non*-continuous model equations are sometimes used, convergence problems are often observed in nonlinear circuit simulation. Another drawback of models having a large number of model parameters is that the extraction procedure can become quite complicated requiring specialized tools that are rather expensive. In this paper we propose a simple, accurate, well converging and easy to extract large-signal model for RF CMOS transistors. The modeling approach we use is from a microwave-engineering point of view, i.e. a set of empirical continuous model equations is used. This approach has been very successful for compact modeling of III-V high frequency transistors and here we *show* that this approach is also viable for Si CMOS transistors. In our work, the proposed model has been implemented and tested in Agilent's ADS and then used to design small- and large-signal circuits.

Drain current

Previously, we have successfully modeled MESFETs and HEMTs using our nonlinear FET model [7]. However, the specifics of the MOSFET require a quite complicated model structure. One of the basic reasons for this is the difference of the saturated velocity dependence vs. electric field in Si in comparison to GaAs, Fig. 1. In GaAs FET devices at some electric field (V_{ds}) we observe a maximum of the carrier velocity&transconductance. In Si we have gradual increase of the carrier velocity, which will produce different shape of I_{ds}, G_m, G_{ds} vs. V_{gs} V_{ds} and the respective parameters that describe these dependences. At small currents the I_{ds} vs. V_{ds} dependence is close to exponential, Fig.2 >logarithmic plots are nearly lines., i.e the model should have also exponential part.

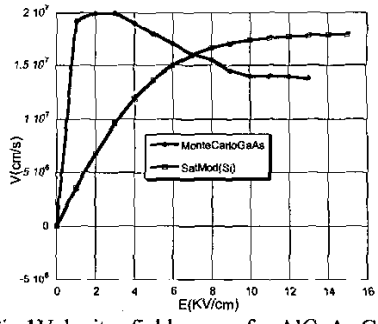

Fig.1 Velocity- field curves for AlGaAs.GaAs &Si

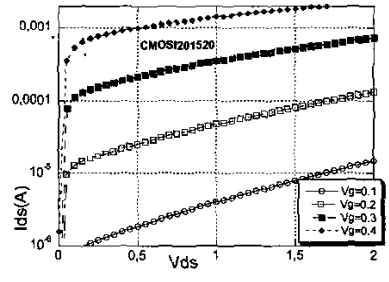

Fig.2 I_{ds} vs. V_{ds} - small current V_{gs} bias.

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These specifics should be addressed if the goal is to have a model working in wide range of voltages and currents. Additional problem is more complicated equivalent circuit, see Fig. 3, and changes and additions to the model reflecting this were required [1-6]. An example is the addition of a bulk terminal together with related components in order to include the bulk effect at very high frequencies. Furthermore, a symmetric description of the drain current is employed for accurate modeling of the transistor behavior for both positive and negative V_{ds}. This is important for devices operating at low drain voltages as well as switches and resistive mixer applications. To obtain this in a proper manner, both V_{gs} and V_{gd} control the current source, respectively:

$$I_{ds} = I_{dsp} - I_{dsn} \ldots (1)$$

$$I_{dsp} = I_{pk}(1+\tanh(\psi_p))(1+\tanh(\alpha_p V_{ds})).$$
$$(1+\lambda_p V_{ds} + \lambda_{1p}\exp(((V_{ds}/V_{kn})-1))) \ldots (2)$$

$$I_{dsn} = I_{pk}(1+\tanh(\psi_n))(1+\tanh(\alpha_n V_{ds})).$$
$$(1-\lambda_n V_{ds} - \lambda_{1n}\exp(((V_{ds}/V_{kn})-1))) \ldots (3)$$

where $\psi_{p,n}$ are power series functions centered at V_{pk}

$$\psi_p = P_{1m}(V_{gs}-V_{pk}) + P_{2m}(V_{gs}-V_{pk})^2 + P_{3m}(V_{gs}-V_{pk})^3 .(4)$$

$$\psi_n = P_{1m}(V_{gd}-V_{pk}) + P_2(V_{gd}-V_{pk})^2 + P_3(V_{gd}-V_{pk})^3 ..(5)$$

$$V_{pk}(V_{ds}) = V_{pks} - \Delta V_{pks} + \Delta V_{pks}\tanh(\alpha_s V_{ds})$$

$$P_{im} = P_i \cdot \Delta P_i \tanh(\alpha_s V_{ds})$$

$$\lambda_i = \lambda - \Delta\lambda \tanh(\psi)$$

$$\alpha_p = \alpha_r + \alpha_s[1+\tanh(\psi_p)]; \alpha_n = \alpha_r + \alpha_s[1+\tanh(\psi_n)]$$

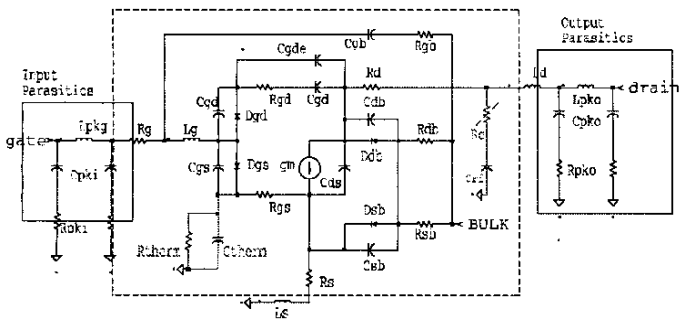

Fig. 3 Equivalent circuit of the transistor.

Typically 3 terms of the power series are enough to produce a model accuracy of 2-5%. V_{pk} and I_{pk} are the gate voltage and the drain current at which the maximum of the trans-conductance occurs, αp, n are the saturation parameters, and the λ parameter accounts for channel length modulation. Some parameters, like V_{pk} and P_1, P_2, P_3,... exhibit V_{ds} dependence and this was accounted for in a similar way as in [7]. The number of parameters for I_{ds} is low (11-14 depending on the requirements)and most of them can be determined directly from measurements. The remaining parameters are extracted using optimization. Our modeling approach thus allows us to use a simple extraction procedure and extracted parameters are trimmed with the default CAD tool optimizers. Fig. 5 shows a good fit between the measured and simulated DC IV data.

Capacitances

In the implementation in ADS, a capacitance formulation was used directly. When the capacitance approach is used, the resulting small-signal equivalent circuit consists of these capacitances evaluated at the corresponding DC voltage.

The small- and large-signal models are consistent and we don't need transcapacitances, because the time derivatives depend only on their own terminal voltage. The problem that can arise using this approach is that as a first step time derivatives should be calculated and harmonic balance (HB) will not converge if the functions for the C_{gs}, C_{gd} are not continuous with well-defined derivatives. In order to account for the specifics of the CMOS device the capacitance equations from [7] are modified to:

$$C_{gs} = C_{gsp} + \frac{C_{gs0}\left(1+V_{gs}+P_{10}\right)}{\sqrt{P_{11}+\left(V_{gs}-P_{10}\right)^2}}\left(1+\tanh\left(P_{20}+P_{20}V_{ds}\right)\right)$$

$$C_{gd} = C_{gdp} + \frac{C_{gd0}\left(1+V_{gs}+P_{40}\right)}{\sqrt{P_{41}+\left(V_{gd}-P_{40}\right)^2}}\left(1+\tanh\left(P_{30}-P_{31}V_{ds}\right)\right) (6)$$

$$I_{gsc} = C_{gs}\frac{\partial V_{gs}}{\partial t}; I_{gdc} = C_{gd}\frac{\partial V_{gd}}{\partial t}; (7)$$

In this case, the selected functions for C_{gs}, C_{gd} are symmetric with well-defined derivatives. This results in a very good convergence behavior in HB.

The drain-source capacitance C_{ds} can be considered constant, for simplicity, but if a more precise model is required, C_{ds} can be modeled as a depletion capacitance with a specially modified equation that converges well at the built-in potential V_{bi} and above.

For circuit simulators that require a charge implementation, our capacitance functions provide integrals solvable in functions available in circuit simulators. Simulated capacitances are shown in Fig.4

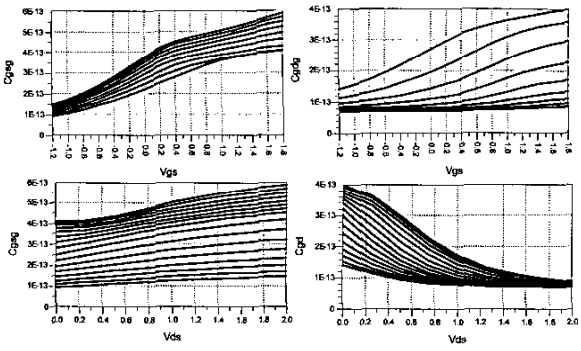

Fig.4. Modeled capacitances.

Thermal effects

To account for the effects of self-heating, in this simple approach only parameters I_{pk}, P_1, C_{gs0} and C_{gd0} are considered. Their temperature dependencies are rather linear versus temperature in the temperature range ± 100°C and are very small. These parameters are modeled generally as:

$$K = K_0(1 + T_{CK}(T_j - T_{ref})) \quad (8)$$

where $K = I_{pk}$, P_1, C_{gs0} and C_{gd0}. T_{CK} is the temperature coefficient of parameter K. The temperature T_j is determined from the total dissipated power and the thermal resistance.

Dispersion modeling

The model structure is organized in such a way that the 4 terminals can be used also to account for dispersion using the back-gate approach. For devices operating in saturation, a simple way to account for the G_{ds} dispersion is to use a parallel branch R_c, C_{rf}, with bias dependent resistor.

$$R_C = R_{C\min} + 1/(1 + 1/R_{C\max} + \tanh(\psi)) \quad (9)$$

Experimental evaluation

MOSFETs from IMEC's 100 nm CMOS process were used for the model evaluation. These devices have typical f_T = 140 GHz and f_{max} = 100 GHz. In order to extract the model parameters, DC, S-parameter (50 MHz to 50 GHz) and PS measurements were performed in our laboratory. The model parameters were extracted using a direct-extraction approach followed by an optimization step using default circuit optimizers in ADS.

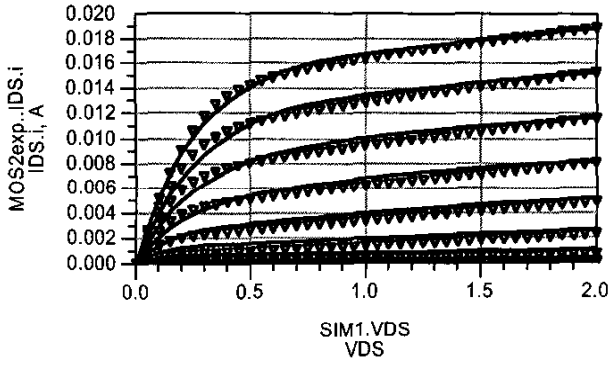

Fig.5 Measured and modeled Ids: Vgs from 0:1v step 0.1V

Fig. 5 shows experimental and modeled I_{ds} characteristics and the agreement is very good. Despite the simplicity of the model the global fit is very good.

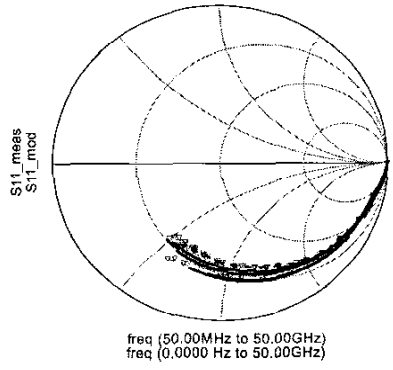

Fig. 6 Measured and modeled S_{11}

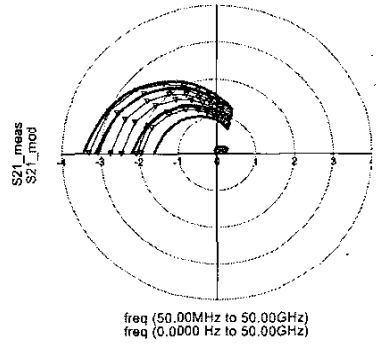

Fig. 7 Measured and modeled S_{21}

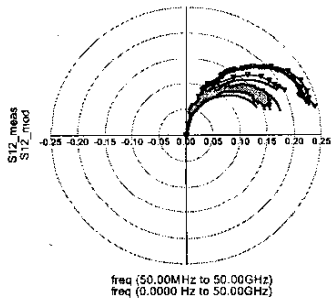

Fig. 8 Measured and modeled S_{12}

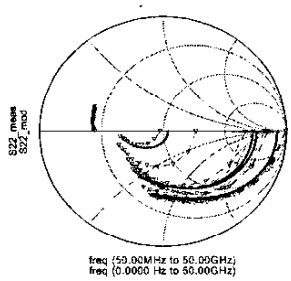

Fig. 9 Measured and modeled S_{22}

Measured and modeled S-parameters, Vgs: 0>1V step 0.5V, Vds:0> 2V step 1V are compared up to 50 GHz and shown in Figs. 6-9. The global fit is good. The starting values for the optimization were obtained by using the method described in [3] and after that, parameters were optimized using directly the CAD tool

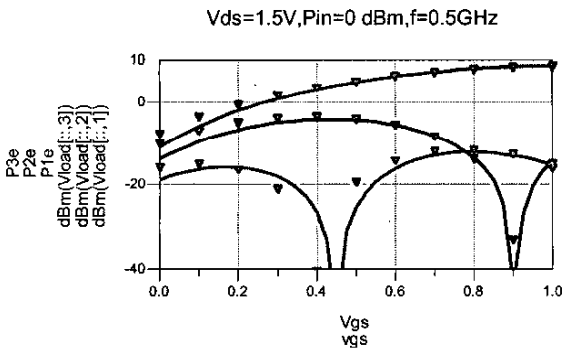

Fig. 10 Measured and modeled PS.

The harmonic content generation was evaluated using PS measurements; see Fig. 10, and a very good global agreement between measured and modeled harmonic content is observed.

Fig. 11 shows measured and modeled P_{out} and gain vs. input power P_{in} at fix bias point and the model describe their dependence very accurately.

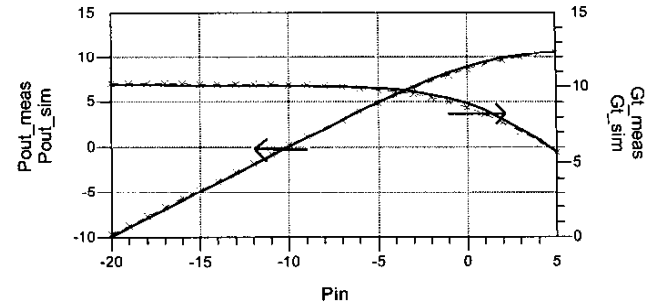

Fig. 11 Measured and modeled P_{out} and gain vs. P_{in}, freq=9GHz, V_{ds}=1.5V, Vgs=0.8V, Z_l=50ohm

Conclusions

A simple large-signal model for high frequency CMOS transistors is proposed, implemented in ADS and experimentally evaluated. The experiments show that our approach for large-signal modeling of state of the art CMOS FETs is feasible and relatively straightforward. The model exhibits very good accuracy and stable behavior in HB simulations. Furthermore, the model is used in practical RF circuit design work.

Acknowledgment

The authors would like to thank the processing group at IMEC for supplying CMOS devices used in the study and support from the IMPACT IST-2000-30016 project. Agilent is acknowledged for the donation of high-frequency simulation software and A. Olausson for the help.

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